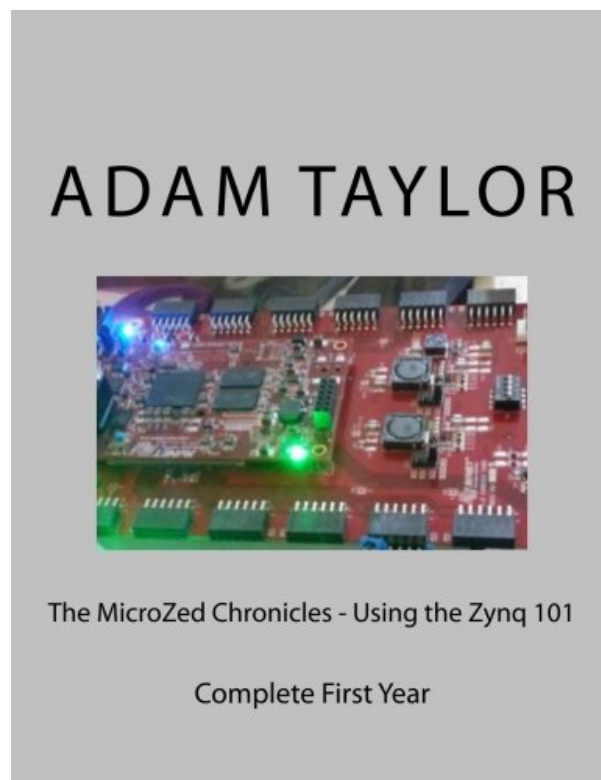


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### About the Author

Adam Taylor is a Chartered Engineer and Fellow of the Institute of Engineering and Technology. He has significant experience working with leading edge defense and space companies where he implemented electronic, FPGA & SoC based solutions to a wide range of areas including Space Telecommunications, RADAR, Cryptography, Image Processing & Safety Critical Control Systems. He has written an extensive number of blogs, papers and presented at a number of conferences over the last 8 years on these subjects. He is passionate about engineering being involved in a number of IEEE committees, University Industry Liaison Boards and being a professional review interviewer for the IET.

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The Xilinx Zynq System on Chip is the SoC in demand at the moment, the MicroZed Chronicles takes you in 52 lessons from the beginning of hello world to creating peripherals within the FPGA and adding in operating systems to make you be able to use the device like a seasoned professional. With over 150 images used to illustrate the lessons and numerous code examples key areas include The Zynq & the SW development environment Configuring the device and generating a boot image XADC & Alarms MIO and EMIO Interrupts including PL to PS Timers, Watchdog both system and Private Triple Timer Counters Creating a AXI Peripheral for the FPGA PS DMA Detailed example of AXI peripheral, SW development Zynq Operating Systems - uc/osiii & FreeRTOS AMP - including communication between cores and SW interrupts

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## Most helpful customer reviews

3 of 3 people found the following review helpful.

Useful, but could be better

By Ed J

I have experience with a ZedBoard and ISE/PlanAhead for Zynq development. I picked up a MicroZed and this book and hoped it would help me make the transition from ISE to Vivado quickly. It is helping, but not quickly.

In general, it is a useful book (I am still working through it), but there are a few issues:

1) The book has no page numbers, but has a table of contents referencing page numbers. However, there are a lot of numbered figures, so the table of figures at the front of the book can be used to infer the page numbers.

- 2) It was written using Vivado 2013.2. I am using a later Vivado and its flow occasionally deviates from the book. I was able to wade through the differences, but it was slow going.
- 3) Some of the figures are critical but unreadable. For example, Figure 29 depicts a modification to the DDR address space in the FSBL loader script, but it is illegible. The supporting text doesn't say what the DDR address address/size values are, but refers to the figure. I went to the online blog from which this book was made, and the same illegible figure is used there. I was able to find the correct values by looking at the linker script of the application created in an earlier step (ps7\_dds\_0\_S\_AXI\_BASEADDR, 0x100000,0x3FF00000)
- 4) Steps to create the boot image were glossed over. It wasn't clear that "datafile" was the necessary partition type for both the FPGA bit file and the standalone C application.

I'm sure I will have a longer list of nitpicks like this, but I am still grateful for the book, especially the later sections that cover topics new to me.

3 of 4 people found the following review helpful.

Getti g a design off the ground was at best challenging. The need to have both fpga confug ...

By DAVID R SPICER

The idea of surrounding a hard wired CPU core with fpga fabtic is not new. Both xilinx and altera have had product offerings with linux support for years. Getti g a design off the ground was at best challenging. The need to have both fpga confug and Cpu software made getting that first "hello world". Up involved many late nights, missed deadlines and loss of hair. I know. I did it the hard way in several designs

The zynq SOC. took this embedded CPU and fpga fabric to a new level, including two ARM9 CPU. Zylinx also included all the usual peripherals we expect on a SOC. Including. Macs, ddr controllers, iic and so on. Just to complicate things more they dumped the old ISE/EDK tool chain and replaced it with a tightly integrated all in one tool called Vivado. The Eclipse based SDK remains pretty much unchanged. All that is to show the scale of the paradigm change in embedded SOC/FPGA. development. a huge amount to take on board for both experienced and new developers. Daunting, to put it mildly.

The used chronicles guide us gently and thoroughly through an apprenticeship in. all these new concepts with lots of examples and pithy explanations. They avoid all the garbage and witty remarks of so many "for dummies" books but never get confusing or obscure.

Xilinx documentation tends to assume the reader has some telepathic ability or connection with the concepts. They are OK and entirely necessary but the used chronicles are a nicely written guide book that makes the perfect complement to the official docs.

Despite many years experience in the cpu/fpga. Design world i would say these books saved me a year on getting up to speed on Xilinx's new direction. In today's world of high pressure design cycles that year simply would have got any commercial project canned. As it is just a few weeks following these texts will bring you right up to speed

Highly recommended. Essential reading in fact.

1 of 2 people found the following review helpful.

Five Stars

By anorman

Excellent information and presentation!!!!

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